UNIVERSITY OF MIAMI

MMI 593 - ADVANCED AUDIO ELECTRONICS

Transistor Power Amplifier with Input Limiter

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CONTENTS

LIST OF FIGURES

1 Specifications and Design

1.1 Specifications

Amplifier was to be designed within the following criteria:

1. Accommodate balanced or unbalanced input
2. Use of discrete transistors for preamp and output driver stages
3. Peak limiter accompanying power amplifier for output protection
4. A maximum of 1 percent THD into 8 ohm loads within 38v supply rails to determine rated power output

1.2 Design Philosophy

The official design criteria for this amplifier were very broad, only requiring that it be high quality, transistor-based, and including dynamics processing. To provide more guidance to the design process and give a practical slant to the project, I added the additional constraint that all operating voltages were to be derived from a spare toroidal transformer I had available, wound to output 28v on its secondaries with 115v input at the primaries, aiding cost-effective construction of the project when time allowed. When rectified, this will yield 38v on the amplifier rails. Inclusion of multiple input sources formats and output protection circuitry further reflects the intent for this design to be realized in hardware and put into use. Component selections were also influenced by size constraints posed in order to have the completed amplifier fit into a standard 1U 19" rack chassis.

1.3 Design Theory and Equations

Though for ease of viewing the amplifier and dynamics processing components of this design are split into separate schematics, they are intended to be combined together and operated as a single unit, with the amplifier operating at a fixed gain and top (open) end of the limiter's threshold adjustment calibrated to keep the amplifier exceeding its rated power output and distortion figures, regardless of the amplitude of the input signal.

Following the dynamics processing subcircuit, the power amplifier's first stage is a differential preamp comprised of a pair of 2N5401 small-signal BJTs, with active current-mirror current sources at both the collector and emitter. Though this stage is differential in design, a single leg of the differential pair is taken as a single-ended output. 6dB of additional gain at this stage could be gleaned from a balanced input driving both legs of the differential amplifier. We can characterize the operation of the this differential amplifier by the following equation:

$$V_{out} = A_d(V_{IN2} - V_{IN1})$$

...where...

$$A_d = B\frac{R_c}{2r_i}$$

Observe that in this circuit IN2 is grounded, which results in the IN1 signal being subtracted from 0v - multiplying the now negative signal present at IN1 by Ad, we observe that the differential preamp is an inverting amplifier.

The power amplifier is running completely open loop with no gain control. Wherever possible collector and emmiter resisters have been replaced with active current sources - these current sources attempt to compensate for the thermal and loading variations which would cause transistor current to fluctuate by providing constant

current regardless of load by mirroring current from one active device to another, and by physical proximity to the heat producing power transistors in the circuit. As the temperature of the power transistors rises, the adjacent current source transistors will follow suit, leading to a shift in bias that matches the shift in current needs in the heated transistors. The current mirror has the additional advantage of being dependent only on a single resistor value for proper operation due to the current from one emitter being mirrored to the other. Precise matching of emitter resistors is not required in this case.

Immediately following the differential preamp, a voltage amplification stage provides the majority of the raw gain in the power amplification. A typical application of small signal transistors as voltage amplifiers is utilized, with the addition of a constant current source as the bias circuit.

The current amplification (and thus final drive) stage of the amplifier is comprised of a Darlington pair in a complimentary output arrangement. Resistors R13 and R14 provide local negative feedback into the first of the Darlington transistors from the second transistor of the pair, compensating for degenerative feedback on the emitter and providing better high frequency stability, at the cost of a mild reduction in gain. The raw theoretical gain of this stage is simply the Beta values for each of the transistors in the pair multiplied together, though common practice usually sees this realized as roughly 80% of the calculated value. An additional parallel driver stage finalizes the output. The parallel output stage is a clone of the second transistor on the Darlington pair, providing additional amplification of the current. R19 and R20 act as summing resistors for the parallel voltages before final output to the loudspeaker.

2 Results

The amplifier design exhibits an overall gain of 91dB from DC to nearly 18khz with a THD of 1%. In full open loop mode, with a line level input signal of 1.228v, the amplifier can drive as much as 90w into a 8 ohm nominal load before encountering the limits of the power supply rails. At this output power, however, the waveform is heavily distorted and the amplifier exhibits 42% THD.

3 Bill of Materials

3.1 Power Amplifier

Item	Quanity	Label-Value	Attributes	Designations
1	1	1uF	RAD0.2	C1
2	2	1N4001	DIODE0.4	D1,D2
3	4	2N5551	TO-92B	Q1,Q6,Q7,Q14
4	2	ECG68	TO-3	Q2,Q15
5	2	ECG388	TO-3	Q3,Q13
6	5	2N5401	TO-92B	Q4,Q5,Q8,Q9,Q12
7	1	ECG189	TO-202	Q10
8	1	ECG188	TO-202	Q11
9	4	1k	AXIAL0.4	R1,R2,R4,R19
10	1	3k	AXIAL0.4	R3
11	4	0.22	AXIAL0.4	R5,R6,R17,R18
12	2	22	AXIAL0.4	R7,R8
13	2	2k	AXIAL0.4	R9,R10
14	1	27.3k	AXIAL0.4	R11
15	1	8	AXIAL0.4	R12
16	2	100	AXIAL0.4	R13,R14
17	1	10k	AXIAL0.4	R15
18	1	500	AXIAL0.4	R16

3.2 PEAK LIMITER

Item	Quanity	Label-Value	Attributes	Designations
1	2	22pF	RAD0.2	C1,C2
2	1	1uF	POLAR0.6	C3
3	2	4.7uF	RAD0.2	C4,C6
4	1	100pF	RAD0.2	C5
5	2	1uF	RAD0.2	C7,C8
6	1	10uF	RAD0.2	C9
7	1	1N914	DIODE0.4	D1
8	1	2N3821	TO-72	Q1
9	2	4.7k var	SIP3	R1,R3
10	1	1000k var	SIP3	R2
11	2	10k	AXIAL0.4	R4,R5
12	1	100k	AXIAL0.4	R6
13	2	1k	AXIAL0.4	R7,R8
14	2	470k	AXIAL0.4	R9,R10
15	1	22k	AXIAL0.4	R11
16	1	1000k	AXIAL0.4	R12
17	2	NE5534	DIP8	U1,U3
18	1	LF356	DIP8	U2

4 Figures and Plots

Figure 4.1: Circuit Schematic, shown without power supply

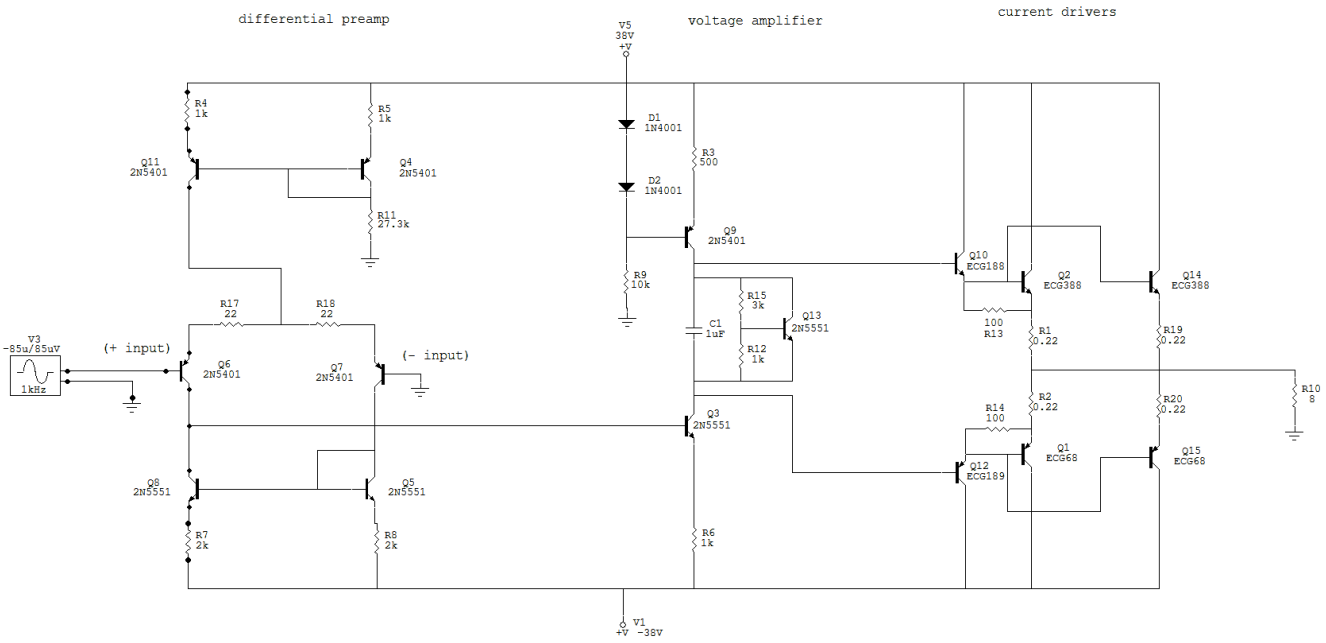

Figure 4.2: Frequency response - Flat to DC with 3db/8ve rolloff at 18khz

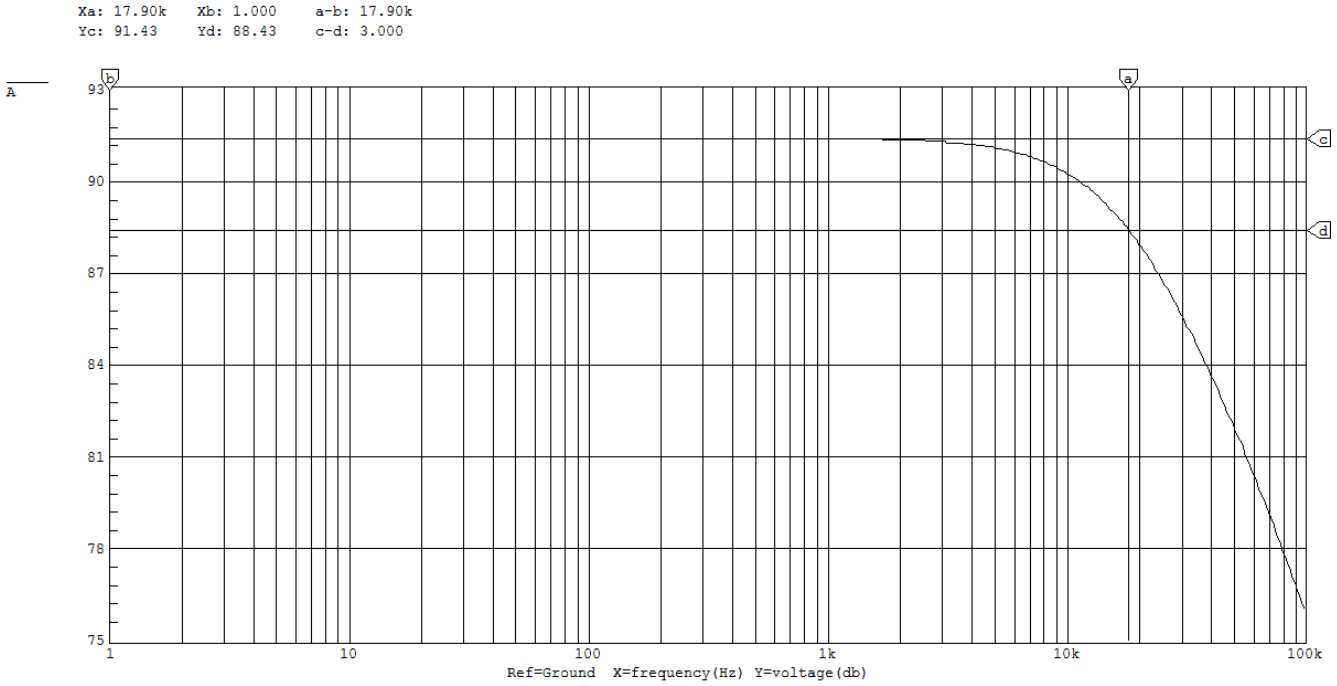

Figure 4.3: Amplified audio waveform, free of clipping or asymmetrical distortion

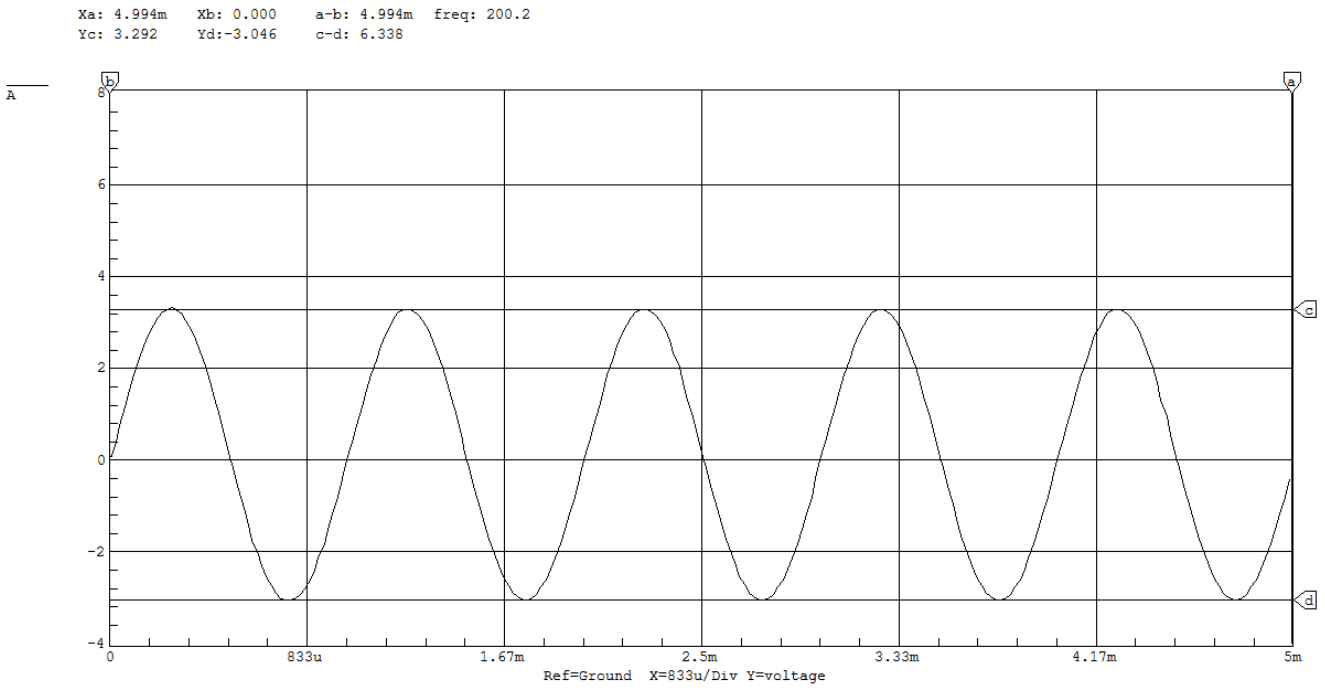

Figure 4.4: Distortion Analysis

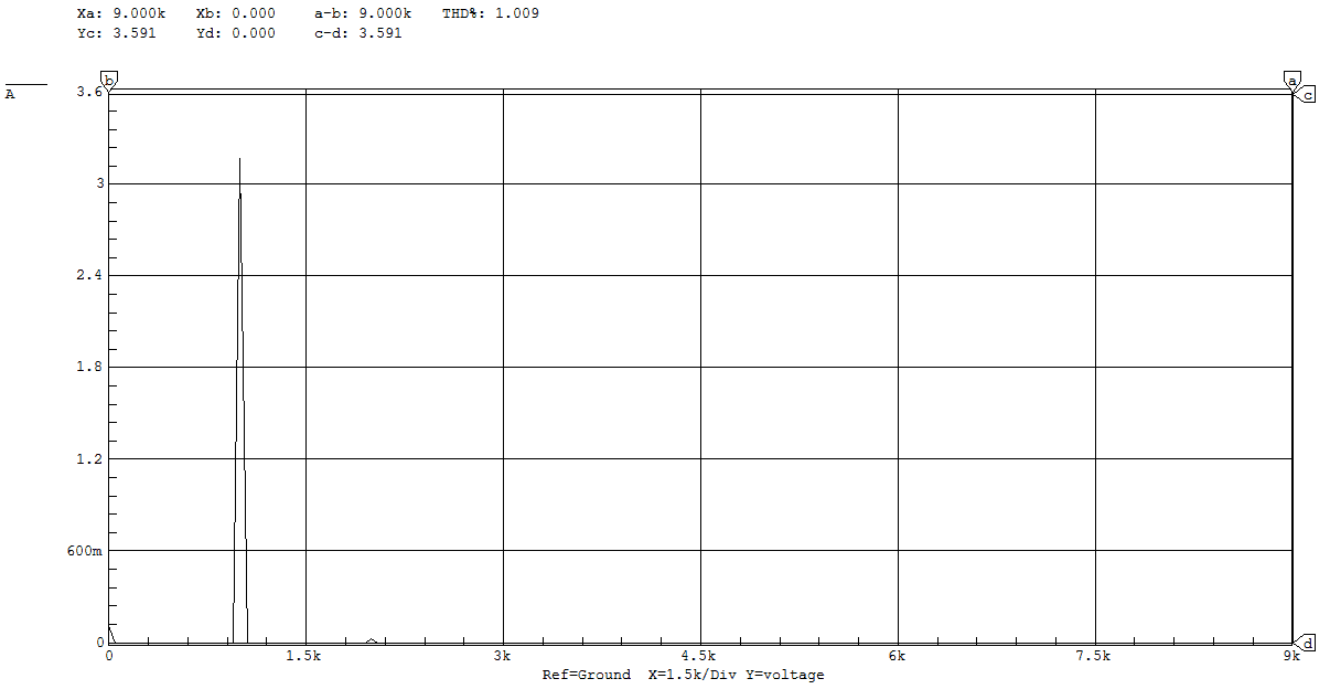

Figure 4.5: Limiter Schematic

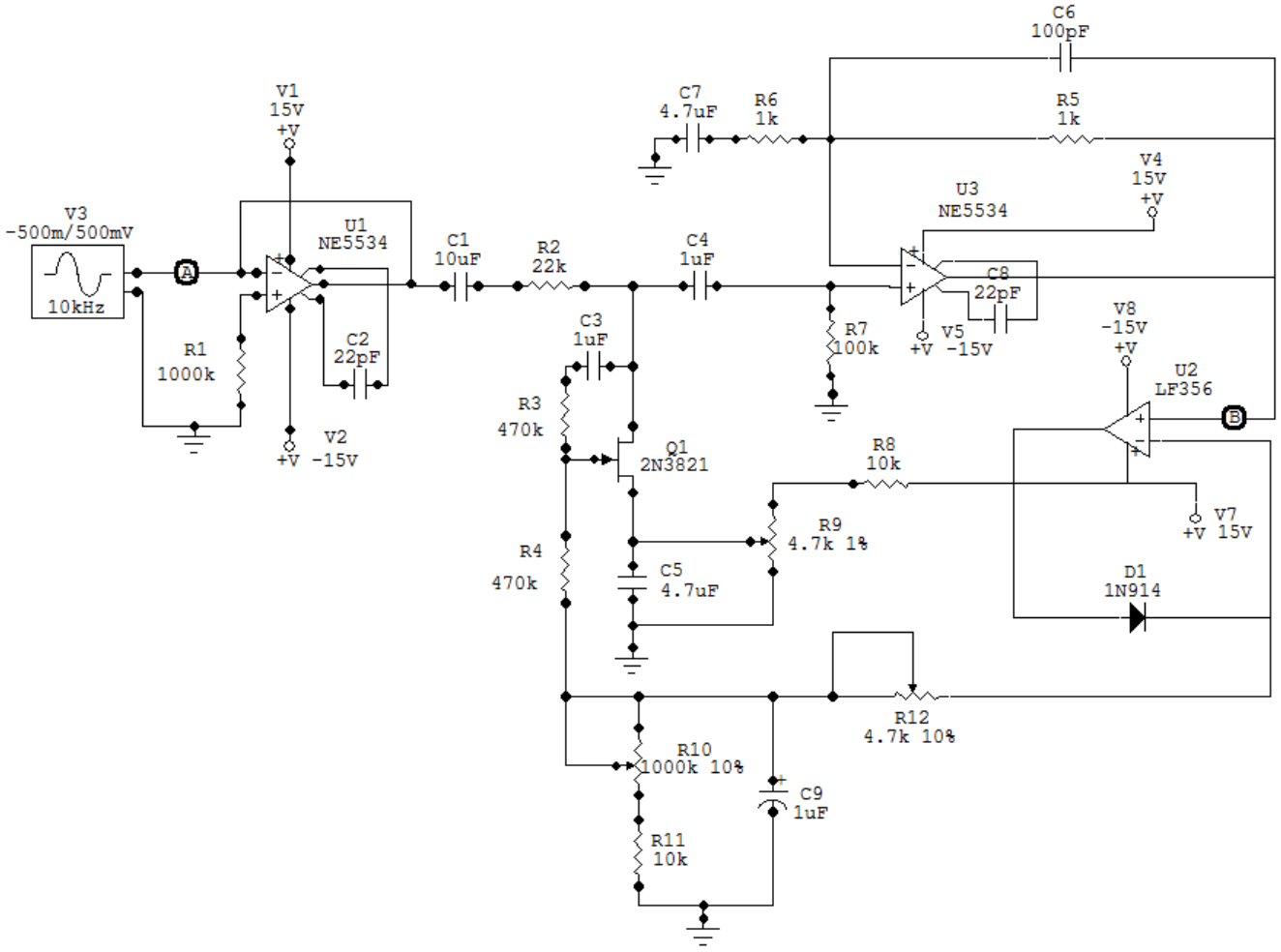

Figure 4.6: Limiter demonstrating extreme "clamping" of signal

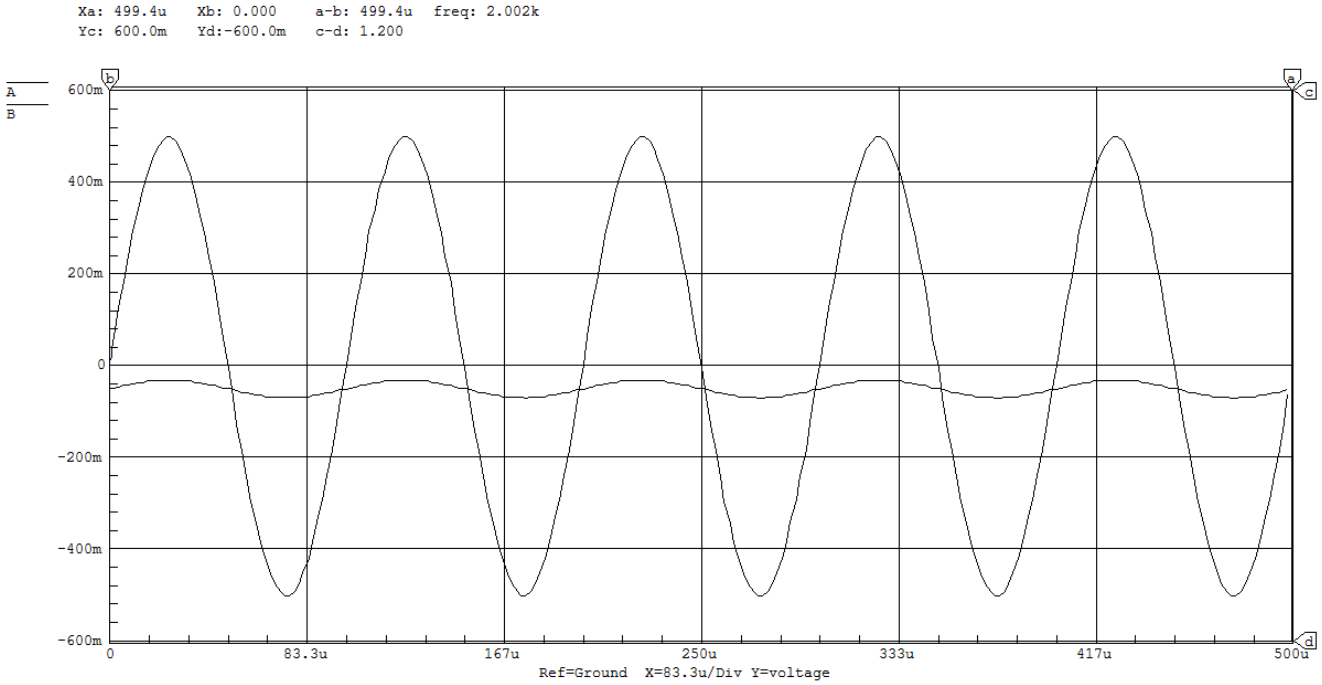

Figure 4.7: Limiter passing signal unimpeded